

Interfacing FlashRunner 2.0 with TEXAS INSTRUMENTS TDA

15/03/2024 Driver v. 5.02 Moreno Ortolan



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TEXAS INSTRUMENTS TDA Introduction

TDA2x SoC for Advanced Driver Assistance Systems (ADAS)

TI's new TDA2x System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS).

The TDA2x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power and ADAS vision analytics processing that aims to facilitate a more autonomous and collision-free driving experience.

The TDA2x SoC enables sophisticated embedded vision technology in automobiles by broadest range of ADAS applications including front camera, park assist, surround view and sensor fusion on a single architecture.

The TDA2x SoC incorporates a heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x digital signal processor (DSP) generation cores, Vision AccelerationPac, Arm[®] Cortex[®]-A15 MPCore[™] and dual-Cortex-M4 processors.

The integration of a video accelerator for decoding multiple video streams over an Ethernet AVB network, along with graphics accelerators for rendering virtual views, enable a 3D viewing experience. And the TDA2x SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision AccelerationPac for this family of products includes multiple embedded vision engines (EVEs) offloading the vision analytics functionality from the application processor while also reducing the power footprint. The Vision AccelerationPac is optimized for vision processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized vision processing.

Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

The TDA2x ADAS processor is qualified according to the AEC-Q100 standard.

PART NUMBER	PACKAGE	BODY SIZE
TDA2SXABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2SGABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2SAABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2HGABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2HVABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2HFABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2LFABC	FCBGA (760)	23.0 mm × 23.0 mm
TDA2Px	FCBGA (760)	23.0 mm × 23.0 mm
TDA2EGABC	FCBGA (760)	23.0 mm × 23.0 mm



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TDA3x SoC for Advanced Driver Assistance Systems (ADAS)

TI's TDA3x System-on-Chip (SoC) is a highly optimized and scalable family of devices designed to meet the requirements of leading Advanced Driver Assistance Systems (ADAS).

The TDA3x family enables broad ADAS applications in automobiles by integrating an optimal mix of performance, low power, smaller form factor and ADAS vision analytics processing that aims to facilitate a more autonomous and collision free driving experience.

The TDA3x SoC enables sophisticated embedded vision technology in today's automobile by enabling the industry's broadest range of ADAS applications including front camera, rear camera, surround view, radar, and fusion on a single architecture.

The TDA3x SoC incorporates a heterogeneous, scalable architecture that includes a mix of Texas Instruments (TI)'s fixed and floating-point TMS320C66x digital signal processor (DSP) generation cores, Vision Acceleration Pac (EVE), and dual-Cortex-M4 processors.

The device allows low power profile in different package options (including Package-On-Package) to enable small form factor designs. TDA3x SoC also integrates a host of peripherals including multi-camera interfaces (both parallel and serial) for LVDS-based surround view systems, displays, CAN and GigB Ethernet AVB.

The Vision Acceleration Pac for this family of products includes embedded vision engine (EVE) offloading the vision analytics functionality from the application processor while also reducing the power footprint.

The Vision Acceleration Pac is optimized for vision processing with a 32-bit RISC core for efficient program execution and a vector coprocessor for specialized vision processing.

Additionally, TI provides a complete set of development tools for the Arm, DSP, and EVE coprocessor, including C compilers, a DSP assembly optimizer to simplify programming and scheduling, and a debugging interface for visibility into source code execution.

The TDA3x ADAS processor is qualified according to AEC-Q100 standard.

PART NUMBER	PACKAGE	BODY SIZE
TDA3LAxABFQ1	FCBGA (367)	15.0 mm × 15.0 mm
TDA3MVxABFQ1	FCBGA (367)	15.0 mm × 15.0 mm
TDA3MAxABFQ1	FCBGA (367)	15.0 mm × 15.0 mm
TDA3MDxABFQ1	FCBGA (367)	15.0 mm × 15.0 mm
TDA3LXxABFQ1	FCBGA (367)	15.0 mm × 15.0 mm





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TEXAS INSTRUMENTS TDA Protocol and PIN map

 $\ensuremath{\text{TDA2}}$ and $\ensuremath{\text{TDA3}}$ devices support the JTAG protocol.

#TCSETPAR CMODE <JTAG>

TEXAS INSTRUMENTS TDA PIN MAP

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																			GND	00							Pin:	B3,	C4						

TEXAS INSTRUMENTS TDA Memory Map

Memory Type	Start Address	End Address	Memory Size	Page Size	Blank Valu	ue Address Unit
[X] – External Memories	0x5C000000	0x5CFFFFFF	16.00 MiB	256	0xFFFFFF	F BYTE
Memory Map Tool Device: TD/ Family: AD/ Manufacturer: TI Algorithm: TD/	\3MV_1x_IS25 \S_3rd_Genera \ - libtda.so	LP128F tion				- D X
Метогу Туре	Start Address *	End Address	Memory Size	Page Size	Blank Value	Address Unit
1 [X] - External Memorie	0x5C000000	0x5CFFFFFF	16.00 MiB	256	0xFFFFFFF	BYTE
		Exp	ort to PDF			
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TEXAS INSTRUMENTS TDA Driver Parameters

The standard parameters are used to configure some specific options inside TDA driver.

#TCSETPAR ENTRY_CLOCK

Syntax:	#TCSETPAR	ENTRY	CLOCK	<frequency></frequency>
Oymax.	#ICSEIFAR	TOIN TIVE	CHOCK	<rrequency></rrequency>

<Frequency> Accepted parameters 4000000, 2000000, 1000000, 500000, 1000000 Hz

 Description:
 Set the JTAG frequency used in the Connect procedure before raising the PLL of the device, if the device PLL is available

Note: Default value 4.00 MHz

#TCSETPAR QSPI_PROTOCOL

Syntax:	#TCSETPAR QSPI_PROTOCOL <value></value>
	<value> Accepted values are SPI and QUAD-SPI</value>
Description:	Use this parameter to set the protocol used to communicate with the external memory connected to TDA3xx device
	The TDA3xx device doesn't support the 4-4-4 QPI mode, so when you set the QUAD-SPI mode, 1-1-4 mode is used for reading from external memory and 1-1-1 for writing into external memory
	In fact, the TDA3x device does not allow you to use writing in 1-1-4 or 4-4-4 1-1-1 means one line for command, one for address, and one for data 1-1-4 means one line for command, one for address, and four for data 4-4-4 means four lines for command, four for address and four for data
	The TDA3xx device doesn't support the DTR - DDR mode (Double Transfer/Data Rate)
Note:	Default value SPI
#TCSETPAR	A OSPI_FREQUENCY
Syntax:	#TCSETPAR QSPI FREQUENCY <value [mhz]=""></value>

<Value [MHz]> Accepted values are 12, 16, 24, 32, 48, 64, 77, 96 and 128 MHz

Description: Use this parameter to set the frequency of SPI - QUAD-SPI used to communicate with the external memory connected to TDA3xx device

Note: Default value 128 MHz

#TCSETPAR QSPI_CHIP_SELECT

Svntax:	#TCSET

#TCSETPAR QSPI CHIP SELECT <Value>

<value></value>	Accepted values are 0, 1, 2 and 3
-----------------	-----------------------------------

Description: Use this parameter to select which chip select you want to use The TDA3xx device has 4 chips select available, so the accepted values of this parameter are 0, 1, 2 and 3

Note: Default value 0

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#TCSETPAR SAMPLING_POINT

Syntax:	#TCSETPAR SAMPLING_POINT <value></value>
	<value> Accepted values are in the range 1-15</value>
Description:	Use this parameter to permanently set the sampling point of the FPGA It is recommended to leave this parameter with the default value

Note: Default value 17

TEXAS INSTRUMENTS TDA Driver Commands

Here you can find the complete list of all available commands for TDA driver.

Memory type:
X → External memory

#TPCMD CONNECT

#TPCMD CONNECT

This function performs the entry and is the first command to be executed when starting the communication with the device.

#TPCMD CONNECT
Protocol selected JTAG.
Entry Clock is 4.00 MHz.
Trying Hot Plug connect procedure.
> Trying to read from ICEPick Module the ID-Code.
* ICEPick rev.D device ID-Code: 0x3BB4C02F.
* Designer: 0x017, Part Number: 0xBB4C, Version: 0x3.
> Trying to read from ICEPick Module the ICEPick Code.
* ICEPick Code: 0x10321AD6.
* Major version: 0x1, Minor version: 0x0.
* Test only taps: 0x3, Emulation taps: 0x2.
* ICEPick type: 0x1AD, Capabilities: 0x6.
> Connecting TAP n.4 Cortex M4 core to ICEPick TAP.
* Cortex M4 IDCODE: 0x4BA00477.
* Designer: 0x23B, Part Number: 0xBA00, Version: 0x4.
* ID-Code read correctly at 4.00 MHz.
* JTAG Debug Port enabled.
> Scanning AP map to find all APs.
* AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.
* AP[0] ROM table base address 0xE00FF000.
> Trying to connect to Arm Cortex M4 core.
* CPUID: 0x410FC241.
* Implementer Code: 0x41 - [ARM].
* Found Cortex M4 revision r0p1.
* Cortex M4 Core halted [0.002 s].
> Trying to use the JTAG frequency inserted by user.
* Requested Clock is 25.00 MHz.
* Generated Clock is 25.00 MHz.
* ID-Code read correctly at 25.00 MHz.
> TDA3xx Cortex M4 Startup Sequence In Progress.
* TDA3xx GP Device detected.
* ID-Code 0x3BB4C02F TDA3x SR2.0A revision 3.
* Found device TDA3MV-FD.
* Package 15x15 FCBGA Lidded, Ball pitch 0.65mm, 367 pins.
* All Control module lock registers unlocked.
> Changing RTI1 reaction type to avoid RTI1 resetting the device.
* Completed change RTI1 reaction type.
Time for Connect: 0.133 s.

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#TPCMD MASSERASE

#TPCMD MASSERASE <X>

Use this command to erase the entire external memory.

#TPCMD ERASE

```
#TPCMD ERASE <X> <4KB>
#TPCMD ERASE <X> <4KB> <start address> <size>
#TPCMD ERASE <X> <32KB>
#TPCMD ERASE <X> <32KB> <start address> <size>
#TPCMD ERASE <X> <64KB>
#TPCMD ERASE <X> <64KB>
#TPCMD ERASE <X> <64KB> <start address> <size>
#TPCMD ERASE <X> <64KB> <start address> <size>
```

Erase external memory with Page/Sector/Block erase.

With this command, a Page/Sector/Block Erase of the external memory will be performed. Typically running the Page/Sector/Block Erase of the external Flash memory takes much longer than running the Masserase command.

Enter the Start Address and Size in hexadecimal format.

#TPCMD BLANKCHECK

```
#TPCMD BLANKCHECK <X>
#TPCMD BLANKCHECK <X> <CRC64>
#TPCMD BLANKCHECK <X> <start address> <size>
#TPCMD BLANKCHECK <X> <start address> <size>
Verify if selected part of an external memory is erased.
The second with CPC64 are usidely for an external memory is that support CPC64 are being and a second seco
```

The two commands with CRC64 are available only for memories that support CRC64 such as MICRON memories. Enter the Start Address and Size in hexadecimal format.

#TPCMD PROGRAM

#TPCMD PROGRAM <X> **#TPCMD** PROGRAM <X> <start address> <size> Program selected part of an external memory. Enter the Start Address and Size in hexadecimal format.

#TPCMD VERIFY

```
#TPCMD VERIFY <X> <R>

#TPCMD VERIFY <X> <R> <start address> <size>

R: Readout Mode.

Verify selected part of an external memory with readout method.

Enter the Start Address and Size in hexadecimal format.
```

```
#TPCMD VERIFY <X> <S>
#TPCMD VERIFY <X> <S> <CRC64>
#TPCMD VERIFY <X> <S> <start address> <size>
#TPCMD VERIFY <X> <S> <start address> <size>
```

S: Checksum 32 Bit Mode.

Verify selected part of an external memory through Checksum 32Bit or CRC64 method. The two commands with CRC64 are available only for memories that support CRC64 such as MICRON memories. Enter the Start Address and Size in hexadecimal format.

#TPCMD READ

#TPCMD READ <X>

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#TPCMD READ <X> <start address> <size> Read selected part of external memory. The result of the read command will be visible into the Terminal. Enter the Start Address and Size in hexadecimal format.

#TPCMD DUMP

#TPCMD DUMP <X>

#TPCMD DUMP <X> <start address> <size>

Dump selected part of external memory. The result of the dump command will be stored in the FlashRunner 2.0 internal memory. Enter the Start Address and Size in hexadecimal format.

#TPCMD CALC_FRB_CRC64

Syntax: #TPCMD CALC_FRB_CRC64

Prerequisites: This command can be used without **#TPCMD** CONNECT

Description: Calculate the CRC64 used for Blankcheck CRC64 and Verify X S CRC64 based on FRB contents

Examples: Correct command execution: 😊

---#TPSETSRC 16MB.frb
>|
---#TPCMD CALC_FRB_CRC64
Verify CRC64 is available only for MICRON memories.
Use the following commands to verify the content of the whole memory:
> Blankcheck:
 #TPCMD BLANKCHECK X 0xB171A45E88C175B7
 #TPCMD BLANKCHECK X 0x5C000000 0x01000000 0xB171A45E88C175B7
> Verify checksum:
 #TPCMD VERIFY X S 0x49757BE6D34FADC9
 #TPCMD VERIFY X S 0x5C000000 0x01000000 0x49757BE6D34FADC9
Time for Calculate CRC64: 0.515 s.

#TPCMD GET_MEMORY_ID

Syntax:	#TPCMD GET_MEMORY_ID
Prerequisites:	none
Description:	Read the external memory ID and print it into Real Time Log and Terminal.
Note:	This command is available from driver version 4.01
Examples:	Correct command execution: 😊
	#TPCMD GET_MEMORY_ID Trying to execute kernel into OCMC RAM. > Kernel init sequence completed. Configured Chip Select n.0. Initialize QSPI peripheral frequency. > QSPI peripheral frequency is 128 MHz. Initialize QSPI GPIO pins.

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#TPCMD RUN

Syntax:	#TPCMD RUN <time [s]=""></time>		
	<time [s]=""></time>	Time in seconds (i.e., 2 s). This time is an optional parameter.	
Prerequisites:	none		
Description:	Move the Reset line up and down quickly if no parameter <time [s]=""> is inserted. #TPCMD RUN <time [s]=""> instead moves the Reset line down, waits for the entered time and then sets the Reset line high. This command typically can be used to execute the firmware programmed in the device.</time></time>		

#TPCMD GET_ID_CODE

Syntax:	#TPCMD GET_ID_CODE
Prerequisites:	none
Description:	Get the TDA device ID Code
Note:	This command prints into Terminal and Real Time Log This command is available from driver version 5.02
Examples:	Correct command execution: 🎯
	Real Time Log:
	#TPCMD GET_ID_CODE Device Id Code: 0x3BB4C02F. * Revision number: 0x3. * Ramp system number: 0xBB4C. * Manufacturer identity (TI): 0x17. * Always set to 1: 0x1. Time for Get ID Code: 0.002 s.

Terminal:

Device Id Code: 0x3BB4C02F

#TPCMD GET_DIE_ID

Syntax:	#TPCMD GET_DIE_ID		
Prerequisites:	none		
Description:	Get the TDA device DIE ID		
Note:	This command prints into Terminal and Real Time Log This command is available from driver version 5.02		
Examples:	Correct command execution: 😌		
	Real Time Log:		
	#TPCMD GET_DIE_ID Device DIE ID 0: 0x1202A00F. Device DIE ID 1: 0x0D5AB3DF. Device DIE ID 2: 0x94954209. Device DIE ID 3: 0x43A40003.		

Terminal:

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Device	DIE	ID	0:	0x1202A00F
Device	DIE	ID	1:	0x0D5AB3DF
Device	DIE	ID	2:	0x94954209
Device	DIE	ID	3:	0x43A40003

#TPCMD GET_PROD_ID

Syntax:	#TPCMD GET_PROD_ID	
Prerequisites:	none	
Description:	Get the TDA device Prod ID	
Note:	This command prints into Terminal and Real Time Log This command is available from driver version 5.02	

Examples:

Real Time Log:

---#TPCMD GET_PROD_ID Device Prod ID: 0x2ED30CF0. Time for Get Prod ID: 0.001 s

Correct command execution: 😊

Terminal:

Device Prod ID: 0x2ED30CF0

#TPCMD GET_DEVICE_TYPE

Syntax:	#TPCMD GET_DEVICE_TYPE
Prerequisites:	none
Description:	Get the TDA device Type
Note:	This command prints into Terminal and Real Time Log This command is available from driver version 5.02
Examples:	Correct command execution: 😳
	Real Time Log:
	#TPCMD GET_DEVICE_TYPE Device Type: 0x000000F8. Time for Get Device Type: 0.001 s.

Terminal:

Device Type: 0x00000F8

#TPCMD READ_MEM8

Syntax:

#TPCMD READ MEM8 <Address> <Byte Count>

	<address> <byte count=""></byte></address>	Address in HEX format (i.e., 0x52002020) Byte count in decimal format (i.e., 8 -> eight bytes)
Prerequisites:	none	
Description:	Read memory byte per byte from target TDA device	

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Note:

This command prints into Terminal and Real Time Log

Examples:

Correct command execution: 😊

#TPCMD READ MEM8 0x52002020	
Read[0x52002020]: 0xF0	
Read[0x52002021]: 0xAA	
Read[0x52002022]: 0x16	
Read[0x52002023]: 0x14	
Read[0x52002024]: 0x00	
Read[0x52002025]: 0x00	
Read[0x52002026]: 0x00	
Read[0x52002027]: 0x00	
Time for Read Mome 0 002 c	

#TPCMD READ_MEM16

Syntax:	#TPCMD READ_MEM16 <address> <16-bit Word Count></address>		
	<address> <16-bit Word Count></address>	Address in HEX format (i.e., 0x52002020) 16-bit Word count in decimal format (i.e., 4 -> four 16-bit words)	
Prerequisites:	none		
Description:	Read memory 16-bit word per 16-bit word from target TDA device		
Note:	This command prints into Terminal and Real Time Log		
Examples:	Correct command execution: 🎯		
	#TPCMD READ_MEM16 0x52002020 4 Read[0x52002020]: 0xAAF0 Read[0x52002022]: 0x1416 Read[0x52002024]: 0x0000 Read[0x52002026]: 0x0000 Time for Read Mem: 0.002 s		

#TPCMD READ_MEM32

Syntax:	#TPCMD READ_MEM32 <address> <32-bit Word Count></address>		
	<address> <32-bit Word Count></address>	Address in HEX format (i.e., 0x52002020) 32-bit Word count in decimal format (i.e., 2 -> two 32-bit words)	
Prerequisites:	none		
Description:	Read memory 32-bit word per 32-bit word from target TDA device		
Note:	This command prints into Terminal and Real Time Log		
Examples:	Correct command execution: 😊		
	#TPCMD READ MEM32 0x52002020 2		

Read[0x52002020]: 0x1416AAF0 Read[0x52002020]: 0x04000000 Time for Read Mem: 0.002 s

#TPCMD DISCONNECT

#TPCMD DISCONNECT

Disconnect function. Power off and exit.

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TEXAS INSTRUMENTS TDA Driver Examples

Here you can see a complete example of TEXAS INSTRUMENTS TDA3 projects.

1 – TEXAS INSTRUMENTS TDA3 example 16MB Commands

TDA3MV_1x_IS25LP128F

TESETPAR ENTRY_LEDGK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR QSPI_CHIP_SELECT 0
#TCSETPAR QSPI_FREQUENCY 128MHz
#TCSETPAR QSPI_PROTOCOL QUAD-SPI
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE JTAG
#TPSETSRC WholeMemory.frb
#TPSTART
#TPCMD CONNECT
#IFERR TPCMD BLANKCHECK X
#THEN TPCMD MASSERASE X
#THEN TPCMD BLANKCHECK X
#TPCMD PROGRAM X
#TPCMD VERIFY X R
#TPCMD VERIFY X S
#TPCMD DISCONNECT
#TPEND

1 – TEXAS INSTRUMENTS TDA3 example 16MB Real Time Log

#TPCMD CONNECT	
Entry Clock is 4.00 MHz.	
Trying Hot Plug connect procedure	
> Trying to read from ICEPick Module the ID-Code	
* ICEPick rev D device ID-Code: 0x3B4C02F	
* Designer: 0x017, Part Number: 0xBR4C, Version: 0x3	
> Trying to read from ICEPick Module the ICEPick Code	
* ICEPick Code: 0x10321AD6	
* Major version: 0x1. Minor version: 0x0.	
* Test only taps: 0x3, Emulation taps: 0x2.	
* ICEPick type: 0x1AD, Capabilities: 0x6	
> Connecting TAP n.4 Cortex M4 core to ICEPick TAP.	
* Cortex M4 IDCODE: 0x4BA00477.	
* Designer: 0x23B, Part Number: 0xBA00, Version: 0x4.	
* ID-Code read correctly at 4.00 MHz.	
* JTAG Debug Port enabled.	
> Scanning AP map to find all APs.	
* AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.	
* AP[0] ROM table base address 0xE00FF000.	
> Trying to connect to Arm Cortex M4 core.	
* CPUID: 0x410FC241.	
* Implementer Code: 0x41 - [ARM].	
* Found Cortex M4 revision r0p1.	
* Cortex M4 Core halted [0.002 s].	
> Trying to use the JTAG frequency inserted by user.	
* Requested Clock is 25.00 MHz.	
* Generated Clock is 25.00 MHz.	
* ID-Code read correctly at 25.00 MHz.	
> TDA3xx Cortex M4 Startup Sequence In Progress.	
* TDA3xx GP Device detected.	
* ID-Code 0x3BB4C02F TDA3x SR2.0A revision 3.	
* Found device TDA3MV-FD.	
* Package 15x15 FCBGA Lidded, Ball pitch 0.65mm, 367 pins.	
> Unlock all Control module lock registers.	
* All Control module lock registers unlocked.	
> Changing RTI1 reaction type to avoid RTI1 resetting the device.	

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* Completed change RTI1 reaction type. Time for Connect: 0.133 s.
Truing to execute kernel into OCMC PAM
Nernel init sequence completed
Configured Chip Select n 0
Initialize OSPI peripheral frequency
> OSPI peripheral frequency is 128 MHz
Initialize OSPI CPIC nins
> OSPI GPIO pins are initialized
Configure OSPI peripheral
> Configured OSPI peripheral
External Memory enter Direct Mode
> Enter Direct Mode completed
Read and check external memory
* OSPI Chip Select 0: Memory ID: Expected 0x18609D - Read 0x18609D
* OSPI Chip Select 0. Status register 0x40
* Clean memory status register
* OSPI Chip Select 0: Status register 0x00.
* OSPI Chip Select 0: SFDP table supported.
* OSPI Chip Select 0: Flash size check passed: 16MiB.
> Completed read and check external memory.
Configure external memory.
* Switching from SPI to OUAD-SPI protocol.
* Set eight dummy cycles.
* Use 3-Byte address mode operation.
> External memory configured.
Execute selected command
External Memory is in Direct Mode.
Time for Blankcheck X: 2.446 s.
#TPCMD PROGRAM X
External Memory is in Direct Mode.
Time for Program X: 16.363 s.
#TPCMD VERIFY X R
External Memory is in Direct Mode.
Time for Verify Readout X: 6.790 s.
#TPCMD VERIFY X S
External Memory is in Direct Mode.
Time for Verify Checksum 32bit X: 2.543 s.

1 – TEXAS INSTRUMENTS TDA3 example 16MB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.133 s
Conditional Blankcheck External Flash	2.446 s
Program External Flash	16.363 s
Verify Readout External Flash	6.790 s
Verify Checksum External Flash	2.543 s
Cycle Time	00:28.370 s

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2 – TEXAS INSTRUMENTS TDA3 example 16MB Commands

TDA3MV_1x_MT25QL128

---#TPSETSRC 16MB.frb

- ---#TPCMD CALC_FRB_CRC64
- Use the following commands to verify the content of the whole memory:
- > Blankcheck:
- * #TPCMD BLANKCHECK X 0x5C000000 0x01000000 0x8171a45E880
- > Verify checksum:
- * #TPCMD VERIFY X S 0x49757BE6D34FADC9
- * #TPCMD VERIFY X S 0x5C000000 0x01000000 0x49757BE6D34FADC
- Time for Calculate CRC64: 0.515 s.

#TCSETPAR ENTRY CLOCK 4000000
#TCSETPAR PROTCLK 37500000
#TCSETPAR PWDOWN 100
#TCSETPAR PWUP 100
#TCSETPAR QSPI CHIP SELECT 0
#TCSETPAR QSPI FREQUENCY 128MHz
#TCSETPAR QSPI PROTOCOL QUAD-SPI
#TCSETPAR RSTDOWN 100
#TCSETPAR RSTDRV OPENDRAIN
#TCSETPAR RSTUP 100
#TCSETPAR VPROG0 3300
#TCSETPAR CMODE JTAG
#TPSETSRC SampleCode_ECUG2_WholeMemory.frb
#TPSTART
#TPCMD CONNECT
#TPCMD BLANKCHECK X 0xB171A45E88C175B7
#TPCMD PROGRAM X
#TPCMD VERIFY X S 0x49757BE6D34FADC9
#TPCMD DISCONNECT
#TPEND

2 – TEXAS INSTRUMENTS TDA3 example 16MB Real Time Log

#TPCMD CONNECT	
Protocol selected JTAG.	
Entry Clock is 4.00 MHz.	
Trying Hot Plug connect procedure.	
> Trying to read from ICEPick Module the ID-Code.	
* ICEPick rev.D device ID-Code: 0x3BB4C02F.	
* Designer: 0x017, Part Number: 0xBB4C, Version: 0x3.	
> Trying to read from ICEPick Module the ICEPick Code.	
* ICEPick Code: 0x10321AD6.	
* Major version: 0x1, Minor version: 0x0.	
* Test only taps: 0x3, Emulation taps: 0x2.	
* ICEPick type: 0x1AD, Capabilities: 0x6.	
> Connecting TAP n.4 Cortex M4 core to ICEPick TAP.	
* Cortex M4 IDCODE: 0x4BA00477.	
* Designer: 0x23B, Part Number: 0xBA00, Version: 0x4.	
* ID-Code read correctly at 4.00 MHz.	
* JTAG Debug Port enabled.	
> Scanning AP map to find all APs.	
* AP[0] IDR: 0x24770011, Type: AMBA AHB3 bus.	
* AP[0] ROM table base address 0xE00FF000.	
> Trying to connect to Arm Cortex M4 core.	
* CPUID: 0x410FC241.	
* Implementer Code: 0x41 - [ARM].	
* Found Cortex M4 revision r0p1.	
* Cortex M4 Core halted [0.002 s].	
> Trying to use the JTAG frequency inserted by user.	
* Requested Clock is 25.00 MHz.	
* Generated Clock is 25.00 MHz.	
* ID-Code read correctly at 25.00 MHz.	
> TDA3xx Cortex M4 Startup Sequence In Progress.	
* TDA3xx GP Device detected.	

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2 – TEXAS INSTRUMENTS TDA3 example 16MB Programming Times

Operation	Timings FlashRunner 2.0
Time for Connect	0.133 s
Conditional Blankcheck External Flash	2.446 s
Program External Flash	16.363 s
Verify Readout External Flash	6.790 s
Verify Checksum External Flash	2.543 s
Cycle Time	00:12.837 s

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TEXAS INSTRUMENTS TDA Driver Changelog

Info about driver version 4.00 - 31/03/2022

Supported TDA3x System-on-Chip (SoC) of Texas Instruments processors. Supported MICRON memories programming via TDA3x device.

Info about driver version 4.01 - 22/04/2022

Supported ISSI memories programming via TDA3x device. Added #TPCMD READ_MEMORY_ID to get the Device ID of an external memory through TDA3xx device.

Info about driver version 4.02 - 16/06/2022

Print current FPGA version loaded into TPSTART command. Upgraded internal code to align all drivers.

Info about driver version 4.03 - 29/06/2022

Connection procedure updated to correctly manage TDA3 boot when valid firmware is present into the external memory connected to the device.

Info about driver version 5.00 - 27/07/2022 Added FPGA for new FlashRunner 2.0 models.

Info about driver version 5.01 - 13/09/2023

Internal driver upgrade.

Info about driver version 5.02 - 15/03/2024

Supported TDA2x System-on-Chip (SoC) of Texas Instruments processors. Added new commands for all TDA devices:

- **#TPCMD** GET_ID_CODE
- **#TPCMD** GET DIE ID
- **#TPCMD** GET PROD ID
- **#TPCMD** GET DEVICE TYPE

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