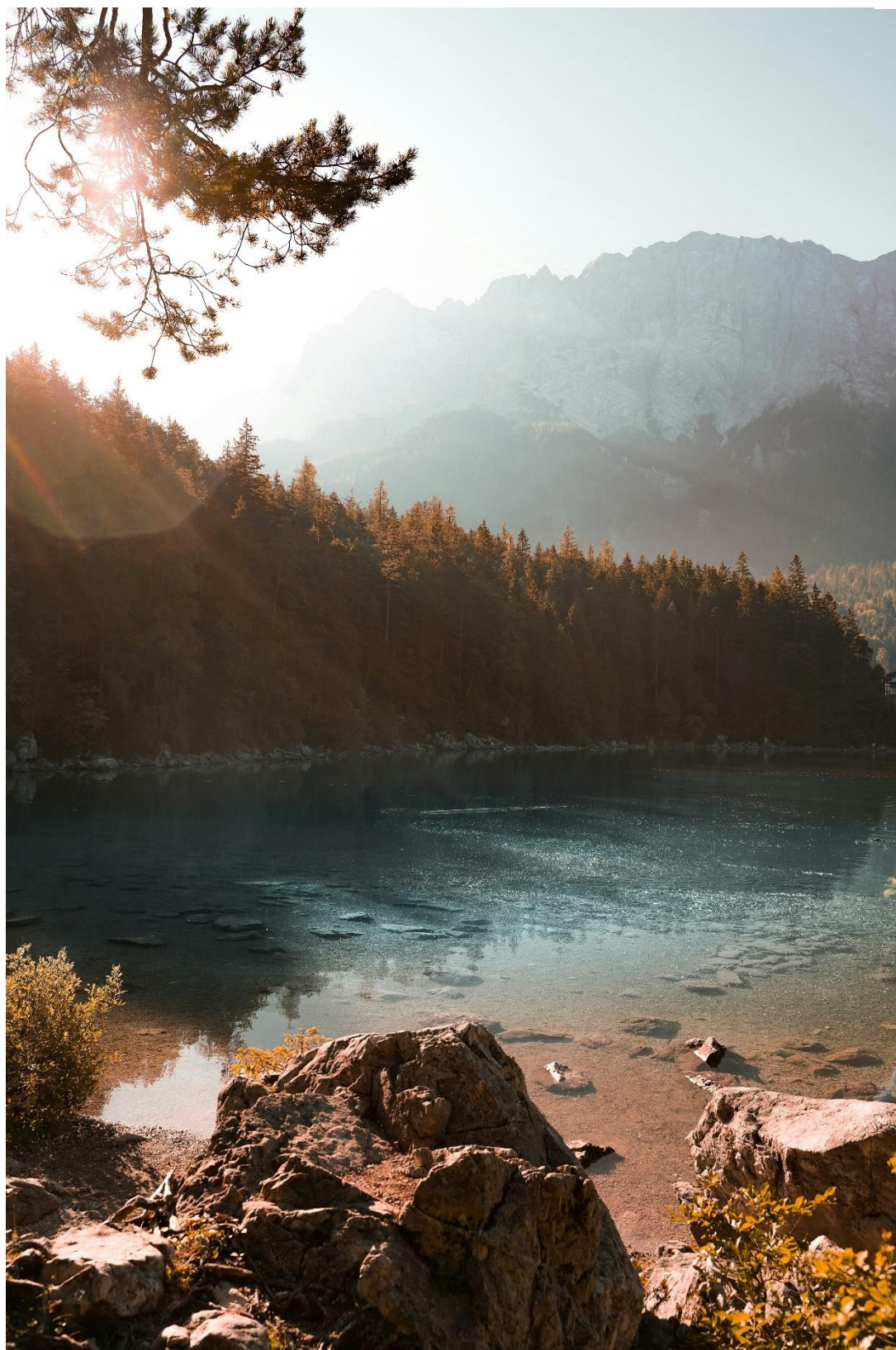


Interfacing FlashRunner 2.0 with TLE98xx



Standard Commands

CONNECT

This command is used to connect to the device. It might print information on the status of the debug interfaces.

MASSERASE <memory_type>

This command is used to erase the specified memory.

SECTOR_ERASE <memory_type> <start_address> <size>

This command is used to erase a portion of the specified memory.

PAGE_ERASE <memory_type> <start_address> <size>

This command is used to erase a portion of the specified memory.

BLANKCHECK <memory_type> [<start_address> <size>]

This command is used to check if the specified memory or a portion of it is blank.

Start address and size are optional parameters.

PROGRAM <memory_type>

This command is used to flash the specified memory with a customer's firmware which fits into this memory.

VERIFY <memory_type> <verify_method>

This command is used to compare the content of the memory with a customer's firmware.

R – Readout method is the one allowed by this algorithm and it compares the content bit by bit.

READ <memory_type> <start_address> <size>

This command is used to read the specified memory or a portion of it and print it out in the GUI terminal.

DUMP <memory_type> <start_address> <size>

This command is used to read the specified memory or a portion of it and save it into a binary file stored inside the programming system SD-CARD.

DISCONNECT

This command is used to disconnect from the device.

Additional Commands

LOCK <password>

LOCK <interface>

This command is used to lock the debug interfaces of the device.

TLE986x/TLE987x require the command to be sent together with a password. (#TPCMD LOCK 0x20)

TLD402x require the command to be sent together with the interface to be locked (SWD|BSL). (#TPCMD LOCK BSL)

All the other devices do not support this command.

UNLOCK <password>

UNLOCK <interface>

This command is used to unlock the debug interfaces of the device.

TLE986x/TLE987x require the command to be sent together with a password. (#TPCMD UNLOCK 0x20)

TLD402x require the command to be sent together with the interface to be locked (SWD).

All the other devices do not support this command.

RUN

This command is used to start customer's application.

VERIFY_CHECKSUM_PAGE <start_addr> <size>

This command is used to verify by checksum a portion of memory.

Only through FastLIN for TLE986x/TLE987x.

NAC_GET

This command is used to retrieve the NAC value programmed into the device.

NAC_SET <value>

This command is used to set the NAC to the specified value.

NAD_GET

This command is used to retrieve the NAD value programmed into the device.

NAD_SET <value>

This command is used to set the NAD to the specified value.

BSL_GET

This command is used to retrieve the BSL value programmed into the device.

BSL_SET <value>

This command is used to set the BSL to the specified value.

PROT_GET <memory_type>

This command is used to retrieve the protection set in the specified memory. The protections could be read-protection, write-protection or both.

PROT_SET <password> <memory_type>

This command is used to set the protection in the specified memory with a password. The protections could be read-protection, write-protection or both.

PROT_CLEAR <password> <memory_type>

This command is used to clear the protection in the specified memory. The password is required to authenticate the process and remove the protections.

Supported protocols

TLE9 flashing algorithm supports both SWD and FastLIN protocols.

```
#TCSETPAR CMODE <SWD>
```

```
#TCSETPAR CMODE <FASTLIN>
```

By keeping the same physical connections, the algorithm is capable of switching protocol in runtime to allow the user to have full access to the microcontroller flashing functionalities in both SWD and FastLIN, when required and possible.

In the following chapters, you will find the full list of supported device families, together with the list of the supported memories and protocols.

Furthermore, it will be explained how to interface the devices that have the double protocol (SWD/FastLIN) when both are required by customers' applications.

At the end, a list of all the flashing commands supported will be explained together with details on the protocol to be used and the families that support those commands.

Additional Parameters

```
#TCSETPAR N_RETRY_ENTRY
```

Used to set the number of attempts to connect to the device.

```
#TCSETPAR ENABLE_FAST_LIN <YES|NO>
```

If set to yes, it allows the usage of the SWD interface of the device even having a FastLIN adapter connected. This is available only for those families that are supported through both interfaces. It is important to follow [this](#) to use SWD with FastLIN adapter.

Protocols and memories

TLE984x family protocols and memories

- Only SWD protocol supported
- Memories supported:
 1. [T] – 100TP
 2. [N] – NACNAD
 3. [F] – Flash
 4. [E] – EEprom

Commands supported:

#TPCMD **CONNECT**

#TPCMD **MASSERASE F**

#TPCMD **BLANKCHECK F** [**<start_address>** **<size>**]

#TPCMD **PROGRAM F | E | T | N** (PROGRAM N requires a FW that has all three NAC/NAD/BSL values inside; refer to single commands to write them singularly (NAD_SET, NAC_SET, BSL_SET))

#TPCMD **VERIFY F | E | T | N R**

#TPCMD **READ F | E** **<start_address>** **<size>**

#TPCMD **DUMP F | E** **<start_address>** **<size>**

#TPCMD **RUN**

#TPCMD **NAC_SET** **<value>**

#TPCMD **NAC_GET**

#TPCMD **NAD_SET** **<value>**

#TPCMD **NAD_GET**

#TPCMD **BSL_SET** **<value>**

#TPCMD **BSL_GET**

#TPCMD **PROT_SET** **<password>** **0 | 1 | 2** (0 for bsl memory segment, 1 for code memory segment, 2 for data memory segment)

#TPCMD **PROT_CLEAR** **<password>** **0 | 1 | 2** (0 for bsl memory segment, 1 for code memory segment, 2 for data memory segment)

#TPCMD **PROT_GET** **0 | 1 | 2** (0 for bsl memory segment, 1 for code memory segment, 2 for data memory segment)

#TPCMD **DISCONNECT**

TLE985x family protocols and memories

- Only SWD protocol supported
- Memories supported:
 1. [N] – NACNAD
 2. [F] – Flash
 3. [E] – Eeprom

Commands supported:

#TPCMD [CONNECT](#)

#TPCMD [MASSERASE F](#)

#TPCMD [BLANKCHECK F](#) [[start_address](#)] [[size](#)]

#TPCMD [PROGRAM F | E | N](#) (PROGRAM N requires a FW that has all two NAC/NAD values inside; refer to single commands to write them singularly (NAD_SET, NAC_SET))

#TPCMD [VERIFY F | E | N R](#)

#TPCMD [READ F | E](#) [[start_address](#)] [[size](#)]

#TPCMD [DUMP F | E](#) [[start_address](#)] [[size](#)]

#TPCMD [RUN](#)

#TPCMD [NAC_SET](#) [[value](#)]

#TPCMD [NAC_GET](#)

#TPCMD [NAD_SET](#) [[value](#)]

#TPCMD [NAD_GET](#)

#TPCMD [DISCONNECT](#)

TLE986x family protocols and memories

- SWD and FastLIN protocols supported
- Memories supported:
 1. [T] – 100TP
 2. [F] – Flash
 3. [E] – Eeprom

Commands supported:

#TPCMD [CONNECT](#) (SWD and FastLIN)

#TPCMD [MASSERASE C](#) (only FastLIN)

#TPCMD [MASSERASE F](#) (SWD and FastLIN)

#TPCMD [SECTOR_ERASE F](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [PAGE_ERASE F](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [BLANKCHECK F](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [PROGRAM F | T | E](#) (SWD and FastLIN)

#TPCMD [VERIFY F | T | E R](#) (SWD and FastLIN)

#TPCMD [VERIFY_CHECKSUM_PAGE](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [READ F | E](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [DUMP F | E](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [LOCK](#) [[entry_delay](#)] [[password](#)] (only FastLIN)

#TPCMD [UNLOCK](#) [[entry_delay](#)] [[password](#)] (only FastLIN)

#TPCMD [RUN](#) (SWD and FastLIN)

#TPCMD [DISCONNECT](#)

**NAC and NAD are contained inside the FLASH memory*

TLE987x family protocols and memories

- SWD and FastLIN protocols supported
- Memories supported:
 1. [T] – 100TP
 2. [F] – Flash
 3. [E] – Eeprom

Commands supported:

#TPCMD **CONNECT** (SWD and FastLIN)
 #TPCMD **MASSERASE C** (only FastLIN)
 #TPCMD **MASSERASE F** (SWD and FastLIN)
 #TPCMD **SECTOR_ERASE F** <start_address> <size> (only FastLIN)
 #TPCMD **PAGE_ERASE F** <start_address> <size> (only FastLIN)
 #TPCMD **BLANKCHECK F** [<start_address> <size>] (SWD and FastLIN)
 #TPCMD **PROGRAM F | T | E** (SWD and FastLIN)
 #TPCMD **VERIFY F | T | E R** (SWD and FastLIN)
 #TPCMD **VERIFY_CHECKSUM_PAGE** <start_address> <size> (only FastLIN)
 #TPCMD **READ F | E** <start_address> <size> (SWD and FastLIN)
 #TPCMD **DUMP F | E** <start_address> <size> (SWD and FastLIN)
 #TPCMD **LOCK** <entry_delay> <password> (only FastLIN)
 #TPCMD **UNLOCK** <entry_delay> <password> (only FastLIN)
 #TPCMD **RUN** (SWD and FastLIN)
 #TPCMD **DISCONNECT**

**NAC and NAD are contained inside the FLASH memory*

TLE988x family protocols and memories

- Only SWD protocol supported
- Memories supported:
 1. [B] – User Bootstrap Loader
 2. [D] – DataFlash
 3. [F] – Flash

Commands supported:

#TPCMD **CONNECT**
 #TPCMD **MASSERASE F | B | D**
 #TPCMD **BLANKCHECK F | B | D** [<start_address> <size>]
 #TPCMD **PROGRAM F | B | D**
 #TPCMD **VERIFY F | B | D R**
 #TPCMD **READ F | B | D** <start_address> <size>
 #TPCMD **DUMP F | B | D** <start_address> <size>
 #TPCMD **RUN**
 #TPCMD **DISCONNECT**

TLE989x family protocols and memories

- Only SWD protocol supported
- Memories supported:
 1. [B] – User Bootstrap Loader
 2. [D] – DataFlash
 3. [F] – Flash

#TPCMD [CONNECT](#)

#TPCMD [MASSERASE F | B | D](#)

#TPCMD [BLANKCHECK F | B | D](#) [[start_address](#)] [[size](#)]

#TPCMD [PROGRAM F | B | D](#)

#TPCMD [VERIFY F | B | D R](#)

#TPCMD [READ F | B | D](#) [[start_address](#)] [[size](#)]

#TPCMD [DUMP F | B | D](#) [[start_address](#)] [[size](#)]

#TPCMD [RUN](#)

#TPCMD [DISCONNECT](#)

TLD402x family protocols and memories

- SWD and FastLIN protocols supported
- Memories supported:
 1. [T] – 1000TP
 2. [F] – Flash

Commands supported:

#TPCMD [CONNECT](#) (SWD and FastLIN)

#TPCMD [MASSERASE F](#) (SWD and FastLIN)

#TPCMD [MASSERASE T](#) (only FastLIN)

#TPCMD [PAGE_ERASE F](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [PAGE_ERASE T](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [SECTOR_ERASE F](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [SECTOR_ERASE T](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [BLANKCHECK F](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [BLANKCHECK T](#) [[start_address](#)] [[size](#)] (only FastLIN)

#TPCMD [PROGRAM F](#) (SWD and FastLIN)

#TPCMD [PROGRAM T](#) (only FastLIN)

#TPCMD [VERIFY F R](#) (SWD and FastLIN)

#TPCMD [VERIFY T R](#) (only FastLIN)

#TPCMD [READ F | T](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [DUMP F | T](#) [[start_address](#)] [[size](#)] (SWD and FastLIN)

#TPCMD [LOCK SWD | BSL](#) (only FastLIN)

#TPCMD [UNLOCK SWD](#) (only FastLIN)*

#TPCMD [RUN](#) (only FastLIN)

#TPCMD [DISCONNECT](#)

*The unlock command can be sent only through FastLIN protocol, so once the BSL (FastLIN interface) has been locked, it is not possible to unlock it. The only interface that remains opened is the SWD, but through this interface it is not possible to send the unlock command.

Hardware connections

For all those commands supported through both interfaces, SWD gives the best timing performances (even ten times faster) by keeping the same stability and reliability of the FastLIN interface.

This is the main reason why it has been studied and developed a way to handle both interfaces maintaining the same physical connections.

Using only SWD (no FastLIN external adapter)

DIOs are the FlashRunner connector lines; SWCLK, RST, SWDIO are the SWD protocol pins of the microcontroller to be connected to the proper FlashRunner connector lines.

TLE984x/TLE985x/TLE986x/TLE987x/TLE988x/TLE989x

Connection descriptions:

DIO1: RST
DIO2: SWCLK
DIO5: SWDIO
VPROG0
GND

TLD402x

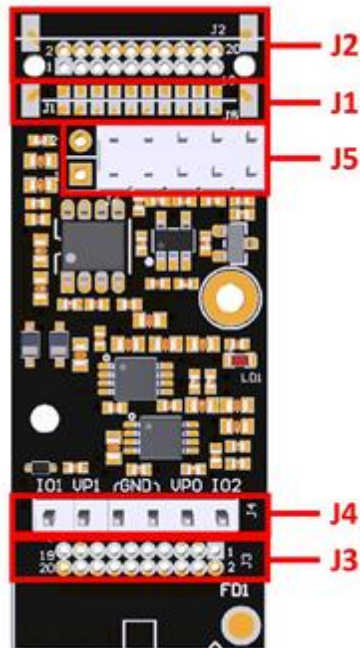
Connection descriptions:

DIO0: Add 1KOhm SWDIO-DIO0
DIO2: SWCLK
DIO5: SWDIO
VPROG0
GND

To use this device it is mandatory to add a 1Kohm resistor between FlashRunner DIO0 and TLD402x SWDIO pin.

Using only FastLIN (valid for all devices supported)

FASTLIN Adapter



Connection from FlashRunner to FastLIN adapter



LIN ADAPTER - J5 CONNECTOR

FlashRunner2.0 Pin Name	FASTLIN adapter connection
GND	J5 - 11
VPROG1	J5 - 5
VPROG0	J5 - 12
DIO1	J5 - 10
DIO2	J5 - 8

Connection from FastLIN adapter to target



Target board Signal Name	Adapter line
GND	J4 – 4
VCC	J4 – 2
LIN	J4 – 6

The adapter needs to be supplied by giving 12V6 to J5 – 3 pin. GND reference J5 – 4 pin.

For TLE986x/TLE987x:

N.B: if lock/unlock features are also needed, POR or HW reset must be guaranteed. This means that either MCU RST pin should be connected to FlashRunner DIO6 or the board should be supplied using VPROG1.

Target board Signal Name	FlashRunner2.0 Pin Name	FASTLIN adapter connection
RST	DIO6	-

If none of this can be achieved, it is not possible to do the following:

- 1) Two following connects command
- 2) Any command after lock
- 3) Any command after unlock

If you need to perform the above things, you must power cycle the board in some other ways, as FLashRunner does not have any chances to do it since of the lack of physical connections (RST or VPROG1).

Using FastLIN and SWD together (adapting SWD to FastLIN external adapter)

FASTLIN Adapter



Connection from FlashRunner to FastLIN adapter and to Target board



LIN ADAPTER - J5 CONNECTOR

Target board Signal Name	FlashRunner2.0 Pin Name	FASTLIN adapter connection
-	GND	J5 – 11
-	VPROG1	J5 – 5
-	VPROG0	J5 – 12
-	DIO1	J5 – 10
-	DIO2	J5 – 8
SWCLK	DIO4	
SWDIO	DIO5	
RST	DIO6	

FlashRunner DIO4, DIO5 and DIO6 are directly connected to the target board signal for the SWD protocol as indicated in the last three entries of the table above.

To use TLD402x, it is mandatory to add a 1Kohm resistor between FlashRunner DIO0 and TLD402x SWDIO pin. RST pin is not available for this device, so DIO6 is not used in this specific family.

Connection from FastLIN adapter to target



Target board Signal Name	Adapter line
GND	J4 - 4
VCC	J4 - 2
LIN	J4 - 6

The adapter needs to be supplied by giving 12V6 to J5 - 3 pin. GND reference J5 - 4 pin.

User cases to switch from SWD to FastLIN and viceversa

The parameter involved in this process are:

- 1) TCSETPAR CMODE <protocol>: defines the protocol for the next set of operations
- 2) TCSETPAR PROTCCLK <frequency>: defines the protocol frequency (115200 fixed for FastLIN)
- 3) TCSETPAR ENABLE_FAST_LIN <yes>: allows the user to use SWD even when the device is connected to the FlashRunner through the FastLIN adapter

Below you can find an example for TLE986x/TLE987x where flashing operations are performed through the SWD protocol and then it switches to FastLIN to lock the debug interface:

```

01 3 | 000101-06:24:28.298 | SWD_CLK: DIO4
01 3 | 000101-06:24:28.298 | SWD_DIO: DIO5
01 3 | 000101-06:24:28.298 | RESET: DIO6
01 2 | 000101-06:24:28.298 | The default FastLIN pin configuration is the following:
01 3 | 000101-06:24:28.298 | LIN_RX: DIO1
01 3 | 000101-06:24:28.299 | LIN_TX: DIO2
01 2 | 000101-06:24:28.299 | >|
01 2 | 000101-06:24:28.299 | ---#TPCMD CONNECT
01 2 | 000101-06:24:28.505 | Protocol clock = 10.00 MHz
01 2 | 000101-06:24:28.505 | Good samples: 11 [Range 0-10].
01 2 | 000101-06:24:28.505 | IDCODE: 0x2BA01477.
01 1 | 000101-06:24:28.505 | Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
01 3 | 000101-06:24:28.505 | Device not locked
01 2 | 000101-06:24:28.507 | >|
01 2 | 000101-06:24:28.507 | ---#TPCMD MASSERASE F
01 1 | 000101-06:24:28.620 | Time for Masserase F: 114 ms
01 2 | 000101-06:24:28.620 | >|
01 2 | 000101-06:24:28.621 | ---#TPCMD BLANKCHECK F
01 1 | 000101-06:24:28.801 | Time for Blankcheck F: 181 ms
01 2 | 000101-06:24:28.802 | >|
01 2 | 000101-06:24:28.802 | ---#TPCMD PROGRAM F
01 1 | 000101-06:24:32.008 | Time for Program F: 3206 ms
01 2 | 000101-06:24:32.008 | >|
01 2 | 000101-06:24:32.008 | ---#TPCMD VERIFY F R
01 2 | 000101-06:24:32.248 | Time for Verify F: 240 ms
01 2 | 000101-06:24:32.248 | >|
01 2 | 000101-06:24:32.248 | ---#TPCMD DISCONNECT
01 2 | 000101-06:24:32.249 | >|
01 2 | 000101-06:24:32.249 | ---#TCSETPAR CMODE FASTLIN
01 2 | 000101-06:24:32.249 | >|
01 2 | 000101-06:24:32.249 | ---#TCSETPAR PROTCCLK 115200
01 2 | 000101-06:24:32.249 | >|
01 2 | 000101-06:24:32.249 | ---#TPCMD CONNECT
01 2 | 000101-06:24:32.459 | Chip ID: 0x68F12E82
01 1 | 000101-06:24:32.471 | Device not locked
01 2 | 000101-06:24:32.471 | >|
01 2 | 000101-06:24:32.471 | ---#TPCMD LOCK 3 0x20
01 1 | 000101-06:24:32.479 | Time for Lock: 8 ms
01 2 | 000101-06:24:32.479 | >|
01 2 | 000101-06:24:32.479 | ---#TPCMD DISCONNECT
01 2 | 000101-06:24:32.479 | >|
01 2 | 000101-06:24:32.479 | ---#TPEND
01 2 | 000101-06:24:32.581 | >|

```

In the remarked part it can be seen the disconnection from the SWD protocol, the parameter change involved to switch to FastLIN and the reconnection with the new protocol to then perform the operations needed.

In the following it is possible to see a double change to unlock the device in FastLIN, flash it in SWD and then lock it in FastLIN again:

```

01 3 000101-06:25:51.551 SWD_CLK: DIO4
01 3 000101-06:25:51.551 SWD_DIO: DIO5
01 3 000101-06:25:51.552 RESET: DIO6
01 2 000101-06:25:51.552 The default FastLIN pin configuration is the following:
01 3 000101-06:25:51.552 LIN_RX: DIO1
01 3 000101-06:25:51.552 LIN_TX: DIO2
01 2 000101-06:25:51.552 >|
01 2 000101-06:25:51.552 ---#TPCMD CONNECT
01 2 000101-06:25:51.761 Chip ID: 0x68F12E82
01 3 000101-06:25:52.062 Device locked
01 2 000101-06:25:52.062 >|
01 2 000101-06:25:52.062 ---#TPCMD UNLOCK 3 0x20
01 2 000101-06:25:52.493 Chip ID: 0x68F12E82
01 1 000101-06:25:52.505 Device not locked
01 1 000101-06:25:52.505 Time for Unlock: 443 ms
01 2 000101-06:25:52.505 >|
01 2 000101-06:25:52.505 ---#TPCMD DISCONNECT
01 2 000101-06:25:52.506 >|
01 2 000101-06:25:52.506 ---#TCSETPAR ENABLE_FAST_LIN YES
01 2 000101-06:25:52.506 >|
01 2 000101-06:25:52.506 ---#TCSETPAR CMODE SWD
01 2 000101-06:25:52.506 >|
01 2 000101-06:25:52.506 ---#TCSETPAR PROTCLOCK 1000000
01 2 000101-06:25:52.506 >|
01 2 000101-06:25:52.506 ---#TPCMD CONNECT
01 2 000101-06:25:52.711 Protocol clock = 10.00 MHz
01 2 000101-06:25:52.712 Good samples: 11 [Range 0-10].
01 2 000101-06:25:52.712 IDCODE: 0x2BA01477.
01 1 000101-06:25:52.712 Designer: 0x23B, Part Number: 0xBA01, Version: 0x2.
01 3 000101-06:25:52.713 Device not locked
01 2 000101-06:25:52.714 >|
01 2 000101-06:25:52.714 ---#TPCMD MASSERASE F
01 1 000101-06:25:52.828 Time for Masserase F: 114 ms
01 2 000101-06:25:52.828 >|
01 2 000101-06:25:52.828 ---#TPCMD BLANKCHECK F
01 1 000101-06:25:53.009 Time for Blankcheck F: 181 ms
01 2 000101-06:25:53.009 >|
01 2 000101-06:25:53.010 ---#TPCMD PROGRAM F
01 1 000101-06:25:56.216 Time for Program F: 3207 ms
01 2 000101-06:25:56.217 >|
01 2 000101-06:25:56.217 ---#TPCMD VERIFY F R
01 2 000101-06:25:56.457 Time for Verify F: 241 ms
01 2 000101-06:25:56.457 >|
01 2 000101-06:25:56.457 ---#TPCMD DISCONNECT
01 2 000101-06:25:56.458 >|
01 2 000101-06:25:56.458 ---#TCSETPAR CMODE FASTLIN
01 2 000101-06:25:56.458 >|
01 2 000101-06:25:56.458 ---#TCSETPAR PROTCLOCK 115200
01 2 000101-06:25:56.458 >|
01 2 000101-06:25:56.458 ---#TPCMD CONNECT
01 2 000101-06:25:56.668 Chip ID: 0x68F12E82
01 1 000101-06:25:56.680 Device not locked
01 2 000101-06:25:56.680 >|
01 2 000101-06:25:56.680 ---#TPCMD UNLOCK 3 0x20
01 1 000101-06:25:56.680 Device not locked
01 2 000101-06:25:56.680 >|
01 2 000101-06:25:56.680 ---#TPCMD DISCONNECT
01 2 000101-06:25:56.680 >|
01 2 000101-06:25:56.681 ---#TPEND

```

The same concept can be applied to other device families that are supported with both interfaces such as TLD402x.